## REMARKS

Claims 1-11 remain in this application. Claims 1and 7 have been amended. The claims 1 and 7 were amended in order to arrange the elements. Claims 1 and 7 were amended to repeat that "bulk CMOS or NMOS" means that there is no buried insulator in the substrate beneath the FETs. This definition of "bulk CMOS or NMOS" is a term of art known to those skilled in the art. Applicants' attorney conducted a "google" search on the Internet for "bulk CMOS." Attached hereto are some of the first articles found in the search. These articles clearly indicate that there is a difference between "bulk CMOS or NMOS" and "SOI" and that bulk CMOS or NMOS does not contain a buried insulator layer. In addition, U.S. Patent No. 6,215,155 B1, col. 1, line 20- col. 2, line17, and Figs. 1 and 2 also nicely state the difference between bulk CMOS/ NMOS and SOI. The bulk CMOS devices used in the examples involved the process of LOCOS in their preparation, page 7, line 21 to page 8, line 2. This process is known by those skilled in the art and involves the surrounding of each FET with a field oxide region. Both bulk CMOS and NMOS recite that the substrate is Si. No new matter has been added.

Inventors Summers and Jackson, and applicants' attorney, Jane Barrow, had a telephone interview with the Examiner on June 18, 2002. Applicants and their attorney wish to thank the Examiner for his granting an interview. Applicants' attorney faxed DRAFT CLAIMS to the Examiner prior to the interview. During the interview, the Examiner indicated that applicants could overcome Terrill et al. by reciting the lack of an insulator layer beneath the FETs. The Examiner indicated that this was a new recitation. Applicants and Applicants' attorney tried to indicate to the Examiner that a "bulk CMOS or NMOS" was not the same as "SOI" semiconductors and that the lack of an insulator layer beneath the FETs in bulk CMOS or NMOS is known to those skilled in the art and therefore the recitation of "bulk CMOS or NMOS" was already in claims 1 and 7.

The drawings were objected to under 37 C.F.R. § 1.83(a). Although the "field oxide region" was described in the specification at page 7, line 21 to page 8, line 2, it was not shown in Fig. 1. Attached hereto is new Fig. 1 showing the field oxide region 24 surrounding the FET to correct the informality. Page 5, second complete paragraph has been amended to add the reference number "24." Support can be found at page 7, line 21 to page 8, line 2, i.e., LOCOS. No new matter is being added.

Claims 1-11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over

Terrill et al. in view of Chen et al.

A prima facie case of obviousness is established when the Examiner provides:

a. References;

b. References that teach;

c. References that are available to the inventors;

d. A suggestion to combine/modify the references; and

e. Evidence that the combination/modification would have made the claimed invention obvious to one of ordinary skill in the art.

In re Wilder, 166 U.S.P.Q. 545, 548 (C.C.P.A. 1970); In re Rinehart, 189 U.S.P.Q. 143, 147 (C.C.P.A. 1976); In re Fine, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); and In re Fritch, 23 U.S.P.Q. 2d 1780, 1783 (Fed. Cir. 1992).

If any one of these elements is not established, then the Examiner's opinion of obviousness is deficient and Applicants are deserving of a patent with respect to this issue, Oetiker, 24 U.S.P.Q.2d 1443, 1447 (Fed. Cir. 1992).

1. References:

The examiner has cited two (2) references, Terrill et al. and Chen et al.

2. References that teach:

The second element requires that the references place the invention in the public domain prior to the date of invention, i.e., the references combine to render the claimed subject matter obvious.

The present invention as recited in claim 1 relates to a bulk CMOS or NMOS device that is resistant to total dose radiation failures due to charge build up in a field oxide. The elements of the device are:

a Si substrate;

one or more FETs on the substrate;

a field oxide region separating each FET; and

a negative voltage source for applying a steady negative back bias to a NMOS region of the substrate to increase the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage in said field oxide region thereby mitigating total dose radiation.

Claim 1 was amended to reiterate that bulk CMOS or NMOS means that there is no insulator buried beneath the FETs. This is the definition known by those skilled in the art as demonstrated by the attached articles from a google search of the Internet and the attached

U.S. Patent No. 6,215,155 B1, col. 1, line 20- col. 2, line17, and Figs. 1 and 2, from a www.uspto.gov search. In both searches, the search term was "bulk CMOS." Although this is a negative limitation, it was already recited in the claim by applicants when using the word "bulk."

The present invention as recited in claim 7 is a method of operating the bulk CMOS or NMOS device to resist total dose radiation due to charge build up in a field oxide through the following steps:

selecting a maximum ionizing radiation dose tolerance for operation of a bulk CMOS or NMOS device (as claimed above); and

determining and applying the negative back bias to the substrate of the NMOS components of the bulk CMOS or NMOS device. The negative back bias is to be sufficient to essentially eliminate leakage currents due to the total dose radiation in the field oxide region of the bulk CMOS or NMOS device thereby providing hardness against maximum ionizing radiation dose.

Applicants' invention is overcoming a problem due to total dose radiation due to a charge build up in the field oxide region. When bulk CMOS or NMOS devices are exposed to total dose radiation, the switches, i.e., transistors, do not shut off and then permanently fail. In order to prevent this failure, a negative back bias is applied that raises the threshold voltage in the field (isolation) region and that tends to shut off radiation-induced parasitic leakage currents, page 5, lines 14-15.

Applicants apply a steady back bias to the NMOS region of the substrate to increase the threshold voltage of the field oxide region to reduce the leakage currents due to the radiation damage in the field oxide region.

Terrill et al. relates to a SOI. The examiner alleges that Terrill et al. "discloses on Fig. 2 substantially all the structure set forth in the claimed invention except a field oxide region separating each FET disposed on a substrate." Terrill et al. does not disclose on Fig. 2 substantially all the structure set forth in the claimed invention. As Terrill et al. relates to an SOI, there is a buried insulator layer 4, Fig. 1 above the Si substrate 6. The Terrill et al. reference is trying to overcome a punchthrough problem due to short-channel effects, Col. 1, line 35-37. The prior art solution to the Terrill et al. problem was solved by increasing the dopant densities, Col. 1, lines 40-52. Terrill et al. solved the problem by providing a means for applying a back-gate bias voltage to induce both charge carriers in the channel region for MOSFET operation and an electric field in the channel region for

restricting punchthrough and other short-channel effects, col. 3, lines 31 to 42, claim 1. Terrill et al. does not have a field effect region for the application of a steady negative back bias as is recited in applicants' amended independent claims 1 and 7.

Chen et al. relates to a SOI. Chen et al. is being cited as it discloses a "field oxide region" separating each FET disposed on a substrate" in Fig. 1. Applicants would like to note that a further examination of Chen et al. reveals that the field oxide region, 38, in Fig. 1 is separated by layer 14, a dielectric material, from layer 12, the substrate. Thus, the FET is not entirely insulated.

If Terrill et al. and Chen et al. were combined, one would not be provided with the claimed invention. Neither of these references relates to bulk CMOS or NMOS. Both of the cited references relate to SOI and therefore have a buried insulator layer. Neither of these references has a field oxide region surrounding each FET in which there is no buried insulator layer. Neither of these references has a negative back bias to the Si substrate beneath the FET in which there is no buried insulator layer. Neither of these references disclose either alone or together the claimed invention. Each of these two references relate to SOI and only an SOI semiconductor. Thus, the second requirement of a prima facie case of obviousness has not been established by the Examiner, and Applicants should be provided with a patent.

3. References that are available to the inventors:

The third element specifies that the references relied upon as prior art be in the inventors' endeavor, or reasonably pertinent to the specific problem in which the inventors were involved, i.e., analogous prior art. In re Antle, 170 U.S.P.Q. 285, 287-88 (C.C.P.A. 1971).

The Federal Circuit has stated in In re Clay, 23 U.S.P.Q.2d 1058, 1060-61 (Fed. Cir. 1992), that:

> [A] reference is reasonably pertinent if...it is one which, because of the matter with which it deals, logically would have commended itself to the inventor's attention in considering his problem... If a reference disclosure has the same purpose as the claimed invention, the reference relates to the same problem... if it is directed to a different purpose, the inventor would accordingly have had less motivation or occasion to consider it.

Neither Terrill et al. nor Chen et al. are analogous prior art as they do not state the same purpose of the present invention which is seeking a method to restrict total dose

radiation that leads to switch failure of bulk CMOS or NMOS devices. Terrill et al. is seeking to prevent punchthrough and other short-channel effects in a SOI. Chen et al. is seeking to overcome the problem of floating gate due to charge accumulation below the channel in SOI. The applicants do not back bias to affect the transistors. Both of these references should be removed as prior art to the determination of a prima facie case of obviousness because neither of the cited reference is reasonably pertinent nor analogous art. Thus, the third requirement of a prima facie case of obviousness has not been established by the Examiner, and Applicants should be provided with a patent.

4. A suggestion to combine/modify the references:

The fourth element requires some reason, suggestion or motivation from the prior art as a whole that indicates that the person of ordinary skill would have combined or modified the references. The Board of Patent Appeals and Interferences has stated in Ex parte Skinner, 2 U.S.P.Q. 2d 1788, 1790 (Fed. Cir. 1987): "When the incentive to combine the teachings of the references is not readily apparent, it is the duty of the examiner to explain why combination of the reference teachings is proper... Absent such reasons or incentives, the teachings of the references are not combinable."

The examiner has stated:

> Regarding claims 1-6, Terrill et al. discloses on figure 2 substantially all the structure set forth in the claimed invention except the field oxide region separating each FET disposed on a substrate. However, Chen et al. discloses on figure 1 a field oxide region 38 separating each FET disposed on a substrate. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Terrill et al. by having a field oxide region separating each FET disposed on a substrate for the purpose of preventing the leakage current from one FET to the other. Office Action dated 03/05/2002, pages 2 and 3.

A disclosure in a figure is not a "teaching." The Federal Circuit stated in In re Fritch, 23 U.S.P.Q.2d 1780, 1783-84 (Fed. Cir. 1992) that:

> "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. Under section 103, teachings or references can be combined *only* if there is some suggestion or incentive to do so." (quoting ACS Hosp. Systems, Inc. v. Montefiore Hosp., 221 U.S.P.Q. 929,933 (Fed. Cir.

1984)) ... The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the invention.

The Board of Patent Appeals and Interferences in In re Regel, Buchel, and Plempel, 188 U.S.P.Q. 136, 139 (BPAI 1975) stated in footnote 6:

> As we have stated in the past, there must be some logical reason apparent from positive, concrete evidence of record which justifies a combination of primary and secondary references. In re Stemniski, supra. Further, as we stated in In re Bergel, 130 U.S.P.Q. (C.C.P.A. 1961):
>
> The mere fact that it is possible to find two isolated disclosures which might be combined in such a way to produce a new compound does not necessarily render such production obvious unless the art also contains something to suggest the desirability of the proposed combination.

The examiner has not directed applicants' attention to a teaching to combine the references. "It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that "one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention". In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Thus, the fourth requirement of a prima facie case of obviousness has not been established by the Examiner, and Applicants should be provided with a patent.

5. Evidence that the combination/modification would have made the claimed invention obvious to one of ordinary skill in the art:

The final element is that the resulting combination or modification appear to show or suggest the claimed invention. None of the cited references in combination appear to suggest the present invention as recited in claims 1-11. The cited references relate to SOI. The present invention relates to bulk CMOS or NMOS. Combine the references and one still would not obtain bulk CMOS or NMOS devices that resist total dose radiation due to charge build up in a field oxide as the present invention does not contain a buried insulator layer beneath the FETs (i.e., neither of the cited references relate to bulk CMOS or NMOS).

There is no teaching or suggestion to combine any of the references. The claimed invention recited in the device and the method claims are not taught. There is no suggestion or teaching of a Si substrate, two or more FETs, a field oxide region separating each FET,

and a negative voltage source for applying a negative back bias to a NMOS region of the substrate to increase the threshold voltage of the field oxide to reduce leakage currents due to radiation damage in said field oxide region thereby mitigating total dose radiation effects. The recited references only relate to SOI and are not solving the problem encountered by the inventors.

The Federal Circuit stated in Oetiker, 24 U.S.P.Q.2d 1449 (Fed. Cir.

It has not been shown that a person of ordinary skill, seeking to solve a problem of fastening a hose clamp, would reasonably be expected or motivated to look to fasteners for garments. The combination of elements from non-analogous sources, in a manner that reconstructs the applicant's invention only with the benefit of hindsight, is insufficient to present a prima facie case of obviousness. There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge can not come from the applicant's invention itself...

Finally, Chen et al. has a field effect region 38 but there is no negative voltage source. Chen et al. does not apply a back bias voltage to the NMOS region of the substrate to raise the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage in the field oxide region. In addition, Chen et al. relates to an SOI.. There is no suggestion or teaching in Chen et al. to combine it with Terrill et al.

Thus, the fifth requirement of a prima facie case of obviousness has not been established by the Examiner, and Applicants should be provided with a patent.

As claims 2-6 depend from amended claim 1 and contain all the limitations of claim 1, it is felt that claims 2-6 distinguish from the cited references in the same manner as amended claim 1. As claims 8-11 depend from amended claim 7 and contain all the limitations of claim 7, it is felt that claims 8-11 distinguish from the cited references in the same manner as amended claim 7.

The test of Section 103 is not whether an improvement or a use set forth in a patent would have been obvious or nonobvious; rather the test is whether the claimed invention, considered as a whole, would have been obvious. Jones v. Hardy, 220 U.S.P.Q. 1021, 1024 (Fed. Cir. 1984). The Federal Circuit in Jones stated:

> Though it is proper to note the differences in a claimed invention from the prior art, because that difference may serve as one element in determining the obviousness/nonobviousness issue, it is improper (even if erroneously

suggested by a party) to consider the difference as the invention. The "difference" may have seemed slight (as has often been the case with some of history's great inventions, e.g., the telephone), but it may also have been the key to success and advancement in the art resulting from the invention. Further, it is irrelevant in determining obviousness that all or all other aspects of the claim may have been well known in the art. Hence the statute, the law established not by judges but by Congress, requires that the invention as claimed be considered "as a whole" when considering whether that invention would have been obvious when it was made. Id. at 1024.

Thus, it is impermissible to focus on the "gist" or "core" of the invention, Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 230 U.S.P.Q. 416, 420 (Fed. Cir. 1986), or on specific differences between the claimed invention and prior art, Jones, at 220 U.S.P.Q. at 1024. Moreover, the invention as a whole is not restricted to the specific subject matter claimed, but also embraces its properties of that structure and the problems which it solves. In re Wright, 6 U.S.P.Q.2d, 1959, 1961 (Fed. Cir. 1988).

Similarly, the references must be taken in their entireties, including those portions which argue against obviousness. Bausch & Lomb, 230 U.S.P.Q. at 420. "It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to a full appreciation of what such reference fairly suggests to one skilled in the art." Id. at 419. The courts have long cautioned that consideration must be given "where the references diverge and teach away from the claimed invention." Akzo N.V. v. International Trade Commission, 1 U.S.P.Q.2d 1241, 1246 (Fed. Cir. 1986).

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In the event that a fee is required, please, charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Respectfully submitted,

, Reg. no. 34,208

John J. Karasek
Reg. No. 36,182
Phone No. 202-404-1552
Associate Counsel (Patents)
Naval Research Laboratory
4555 Overlook Avenue, SW
Washington, D.C. 20375-5325

Prepared by:
Jane Barrow
Reg. No. 34,217
Phone No. 202-404-1551

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Drawings:

New Fig. 1 has been attached hereto.

In the Specification:

The specification at page 5, second complete paragraph has been amended as follows:

The negative bias source 22 is adapted for applying a steady negative back bias to the substrate at a voltage that mitigates total dose radiation failures. The device operates by mitigating leakage currents about the device, while allowing the device to operate within its operational range, i.e., without changing the threshold voltage of the device to a degree that will cause the device to operate poorly. Typically, this negative bias will be between about -3V and about -0.5 V, relative to the source. The inventors have recognized that in the current generation of commercial CMOS devices, total dose radiation failures arise in the isolation region 24, rather than in the gate region.

In the claims:

Claim 1 has been amended as follows:

1. (Twice Amended) A bulk CMOS or NMOS device [having two or more FETs and having a field oxide region separating each FET which are disposed on a substrate, the device being] resistant to total dose radiation failures due to charge build up in a field oxide, the device [further] comprising:

a Si substrate;

two or more FETs on said substrate;

a field oxide region separating each FET; and

a negative voltage source[,] for applying a steady negative back bias to a NMOS region of said substrate to increase the threshold voltage of the field oxide region [in a NMOS field oxide region] to [mitigate] reduce leakage currents [in said device,] due to radiation damage in said field oxide region thereby mitigating total dose radiation effects,

[wherein said field oxide region separates each FET] and

wherein a bulk CMOS or NMOS device does not include an insulator layer beneath said FETs.

Claim 7 has been amended as follows:

7. (Twice Amended) A method for operating a bulk CMOS or NMOS device to resist total dose radiation effects due to charge build up in a field oxide,

[said CMOS or NMOS device having two or more FETs with a field oxide region separating each FET disposed on a substrate,] said method comprising the steps of:

selecting a maximum ionizing radiation dose for operation of said bulk CMOS or NMOS device, wherein said bulk CMOS or NMOS device comprises a Si substrate; two or more FETs on said substrate; a field oxide region separating each FET; and a negative voltage source for applying a steady negative back bias to a NMOS region of said substrate to increase the threshold voltage of the field oxide region to reduce leakage currents due to radiation damage in said field oxide region thereby mitigating total dose radiation effects, and wherein a bulk CMOS or NMOS device does not include an insulator layer beneath said FETs; and

determining and applying [a] said negative back bias to said substrate of NMOS components of said bulk CMOS or NMOS device, wherein said negative back bias is sufficient to essentially eliminate leakage currents due to total dose radiation in said field oxide region of said CMOS or NMOS device[,] thereby providing hardness against said maximum ionizing radiation dose.

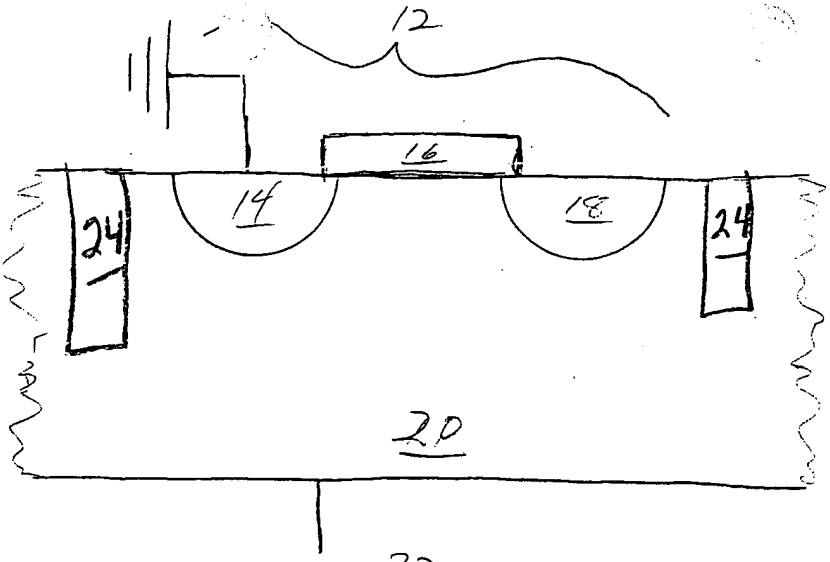


FIG. 1